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FACSIMILE COVER SHEET

To: Commissioner for Patents	Total Pages Sent: 3
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Facsimile Number: (571) 273-2885	Transmission Date: November 2, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Schloesser, *et al.* Docket No.: INF-135
Serial No: 10/777,128 Art Unit: 2818
Date Filed: February 13, 2004
Title: Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at (571) 273-2885 on the date shown above:

- Certification of Facsimile Transmission (1 page)
- Submission Of Papers Cited In Background Section (1 page)
- Copy of 1st page of U.S. Patent No. 6,352,894 B1 (1 page)

Respectfully submitted,

Kristin R. Hayes
Legal Assistant

Confirmation Respectfully Requested

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Serial No.: 10/777,128 Art Unit: 2818
Filed: February 13, 2004 Examiner: Huynh, Andy
For: Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF PAPERS CITED IN BACKGROUND SECTION

Dear Sir:

Applicants provide herewith the first page of U.S. Patent No. 6,352,894 B1 that is cited in the above-referenced application. Since this patent is not material to the patentability of any of the claims, Applicants believe that examination of this reference is not necessary. However, since this patent was cited in the background, Applicants request that a copy be placed in the file.

Respectfully submitted,

Ira S. Matsil
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November 2, 2005

Date

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